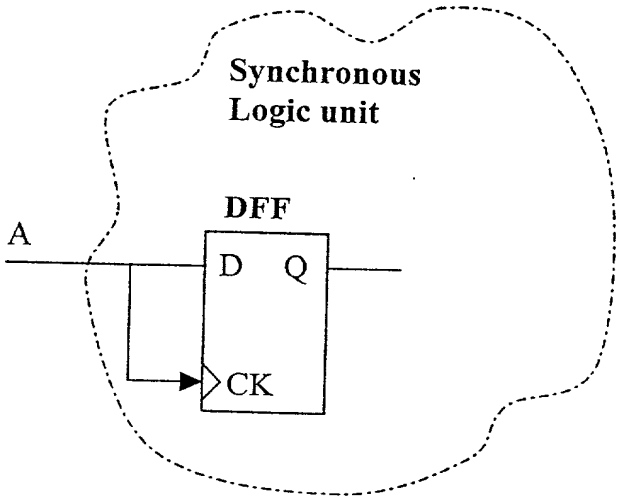


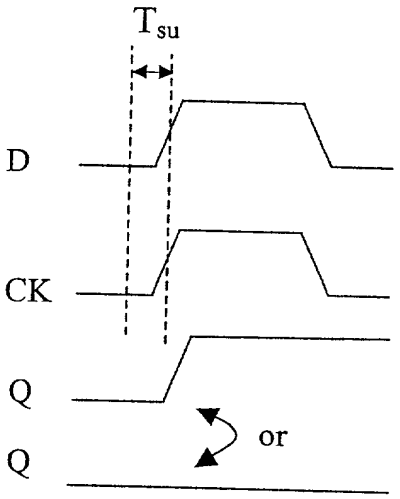
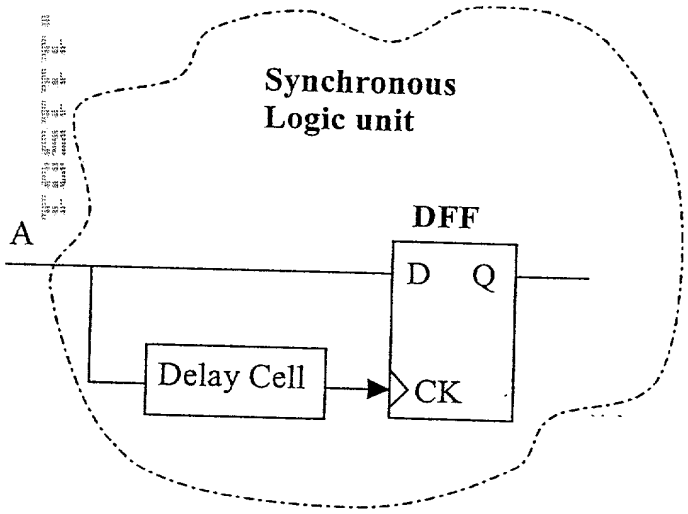


FIGURE 1A



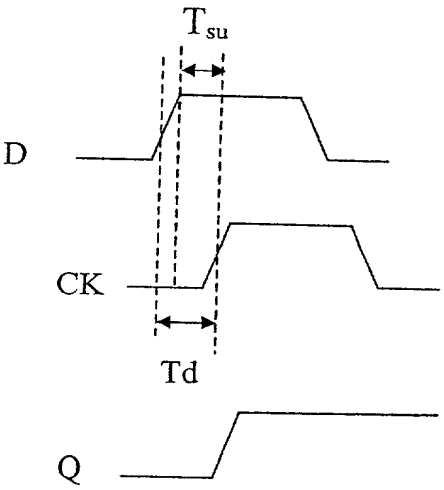


FIGURE 1B

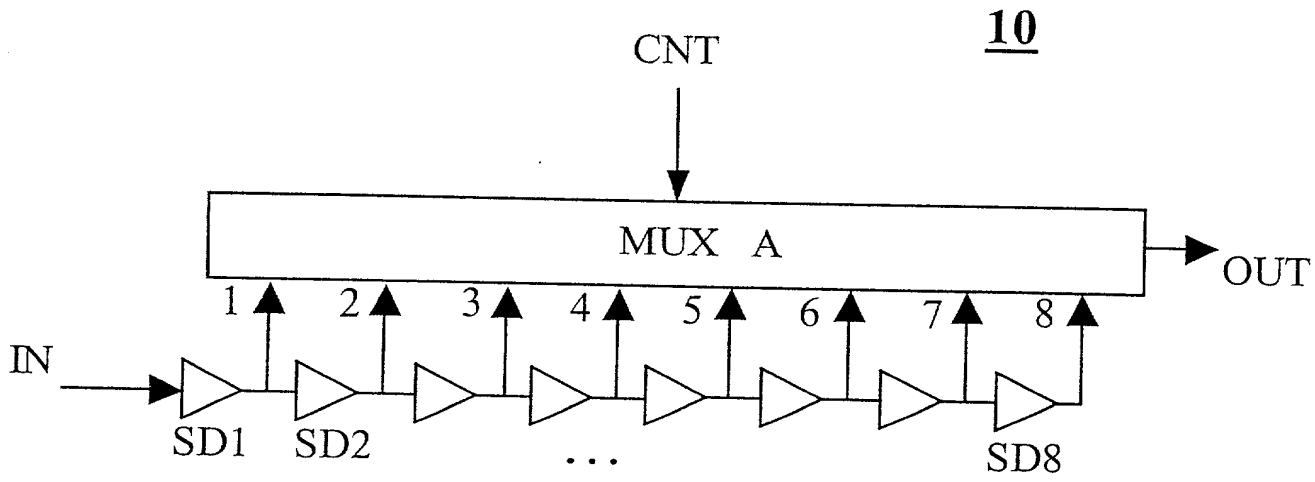


FIGURE 2

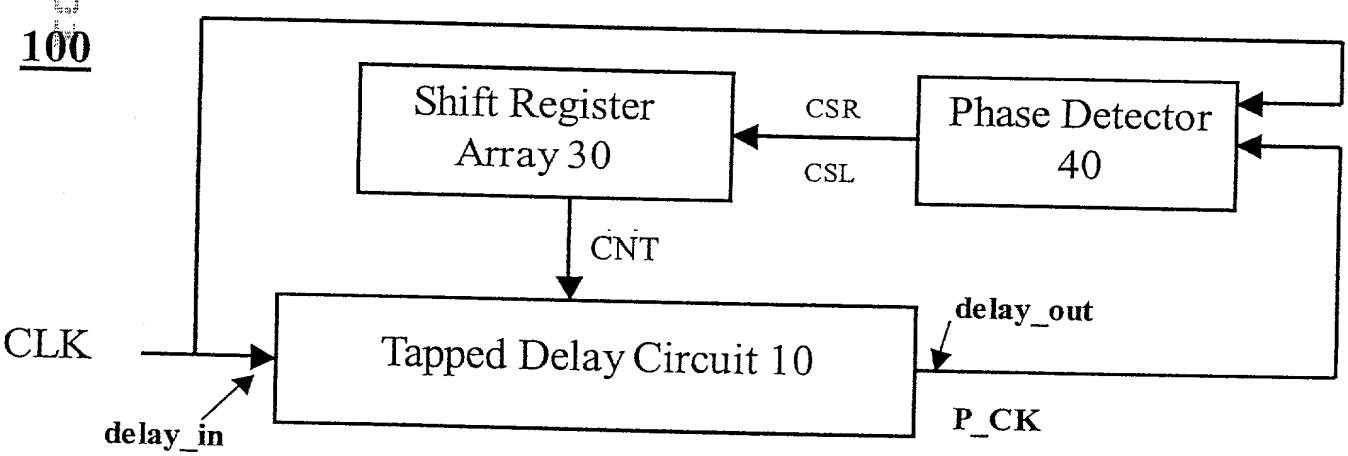


FIGURE 3

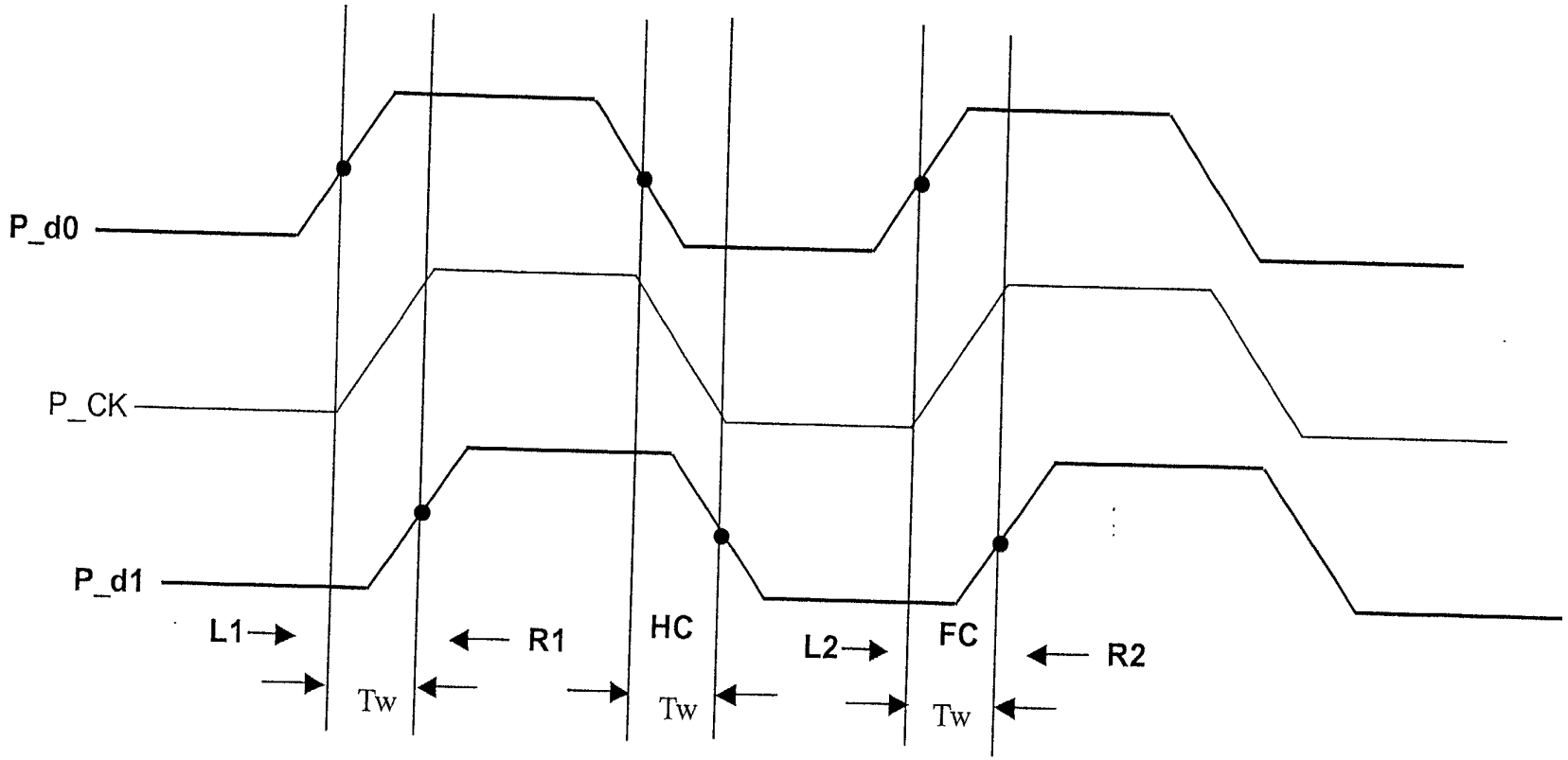


FIGURE 4

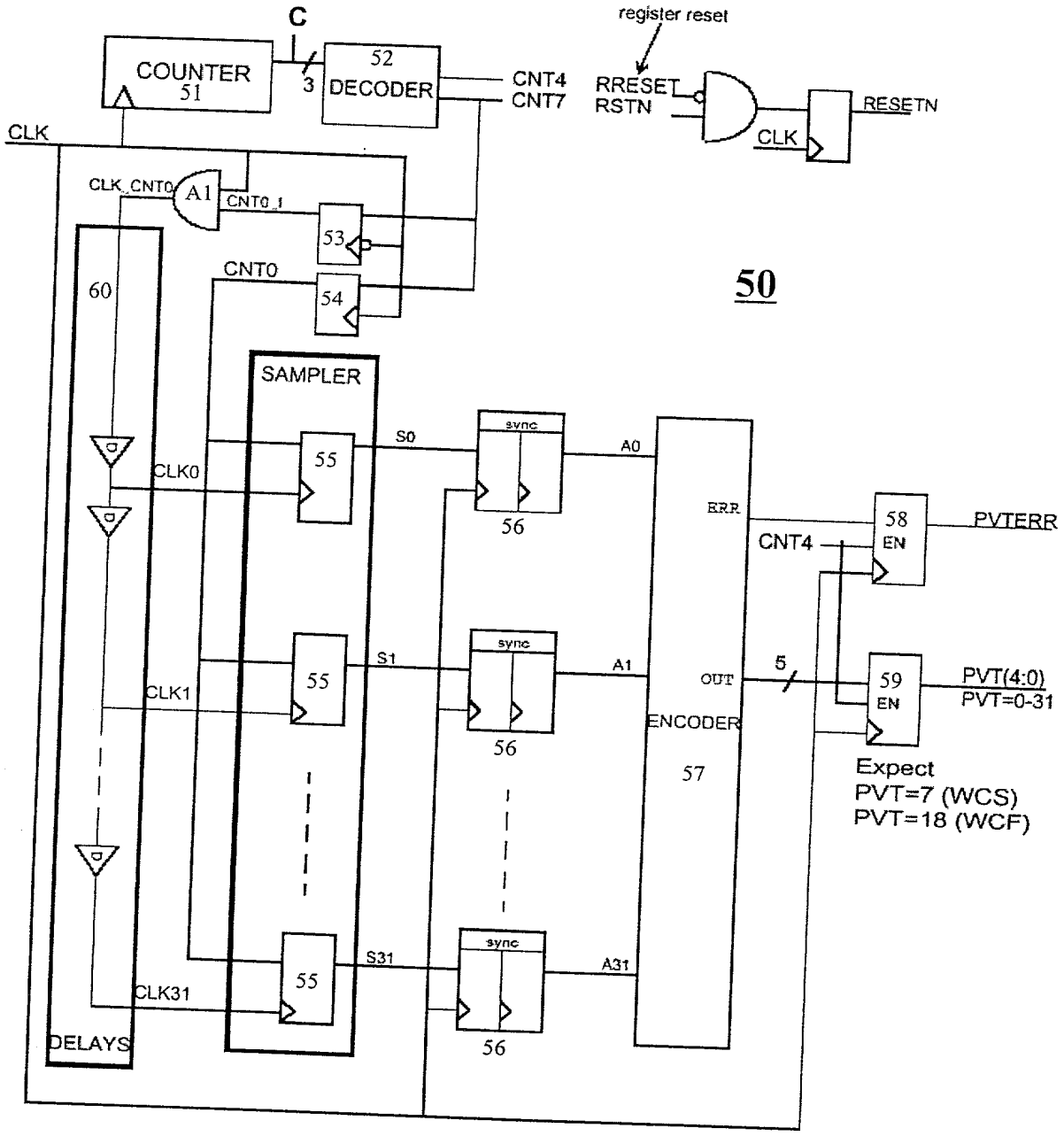

C
COUNTER
51
3
52
DECODER
CNT4
CNT7
register reset
RRESET
RSTN
RESETN
CLK
CLK_CNT0
A1
CNT0_1
53
CNT0
54
50
60
SAMPLER
55
S0
sync
56
A0
CLK0
ERR
58
EN
PVTERR
CNT4
S1
A1
CLK1
OUT
5
59
EN
PVT(4:0)
PVT=0-31
ENCODER
57
Expect
PVT=7 (WCS)
PVT=18 (WCF)
S31
A31
CLK31
DELAYS

FIGURE 5

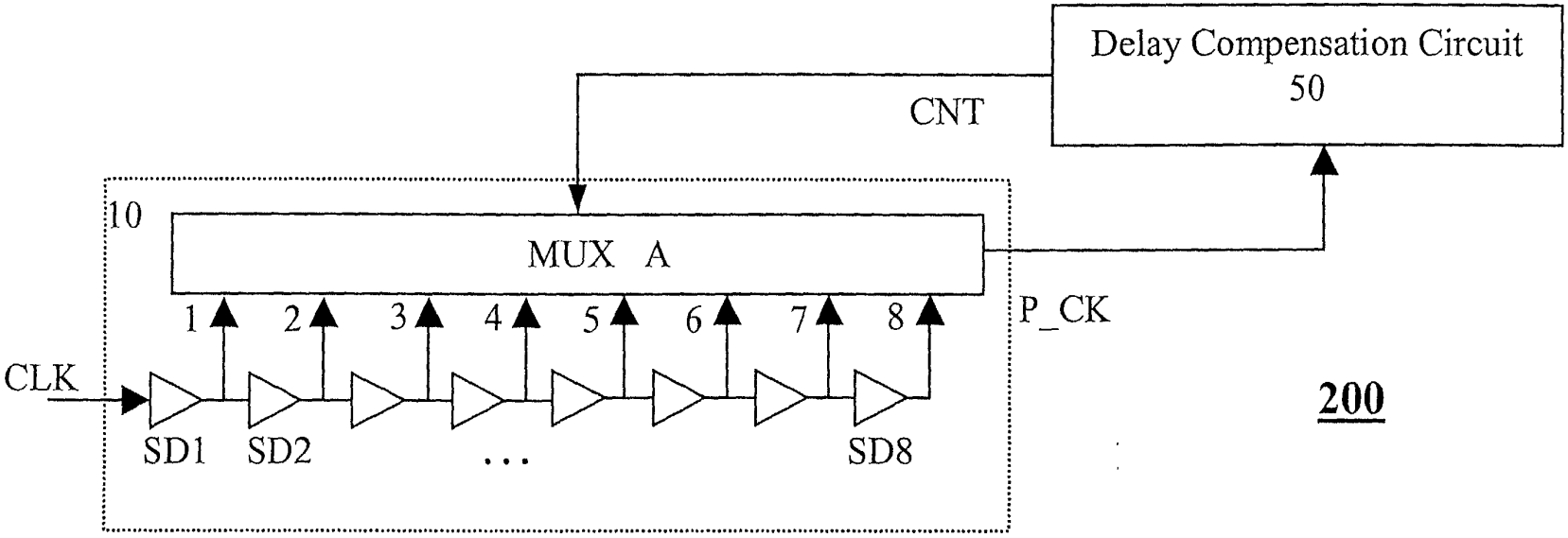


FIGURE 6

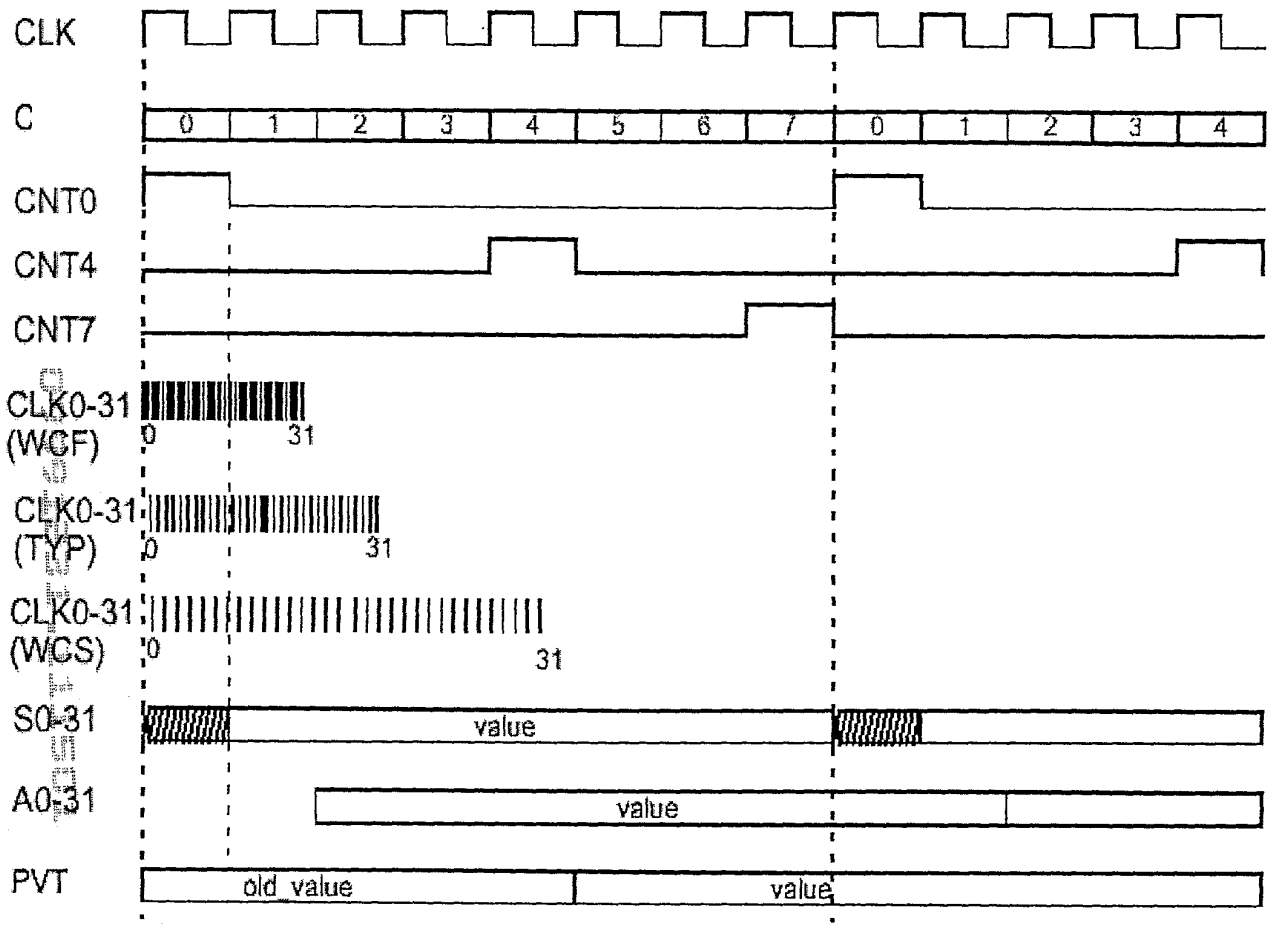

CLK
C
0
1
2
3
4
5
6
7
0
1
2
3
4
CNT0
CNT4
CNT7
CLK0-31
(WCF)
0
31
CLK0-31
(TYP)
0
31
CLK0-31
(WCS)
0
31
S0-31
value
A0-31
value
PVT
old_value
value

FIGURE 7

Expected Synchronizer Outputs for Worst Case Fast and Worst Case Slow Conditions of DELC1V15 Delay Chips

n	CLK*n*	Number of delays for CLK*n*	WCF		WCS	
			delay (ns)	S*n*	delay (ns)	S*n*
0	CLK0	1	0.4	1	1.0	1
1	CLK1	2	0.8	1	2.0	1
2	CLK2	3	1.2	1	3.0	1
3	CLK3	4	1.6	1	4.0	1
4	CLK4	5	2.0	1	5.0	1
5	CLK5	6	2.4	1	6.0	1
6	CLK6	7	2.8	1	7.0	1
7	CLK7	8	3.2	1	8.0	0
8	CLK8	9	3.6	1	9.0	0
9	CLK9	10	4.0	1	10.0	0
10	CLK10	11	4.4	1	11.0	0
11	CLK11	12	4.8	1	12.0	0
12	CLK12	13	5.2	1	13.0	0
13	CLK13	14	5.6	1	14.0	0
14	CLK14	15	6.0	1	15.0	0
15	CLK15	16	6.4	1	16.0	0
16	CLK16	17	6.8	1	17.0	0
17	CLK17	18	7.2	1	18.0	0
18	CLK18	19	7.6	0	19.0	0
19	CLK19	20	8.0	0	20.0	0
20	CLK20	21	8.4	0	21.0	0
21	CLK21	22	8.8	0	22.0	0
22	CLK22	23	9.2	0	23.0	0
23	CLK23	24	9.6	0	24.0	0
24	CLK24	25	10.0	0	25.0	0
25	CLK25	26	10.4	0	26.0	0
26	CLK26	27	10.8	0	27.0	0
27	CLK27	28	11.2	0	28.0	0
28	CLK28	29	11.6	0	29.0	0
29	CLK29	30	12.0	0	30.0	0
30	CLK30	31	12.4	0	31.0	0
31	CLK31	32	12.8	0	32.0	0
PVT (Total A*n*)				18		7

FIGURE 8

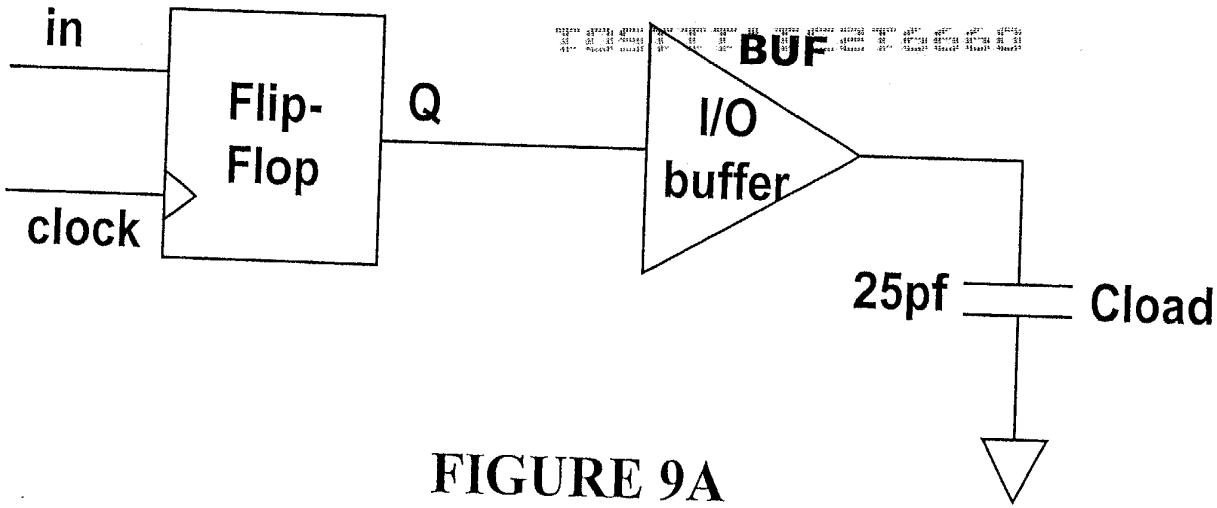


FIGURE 9A

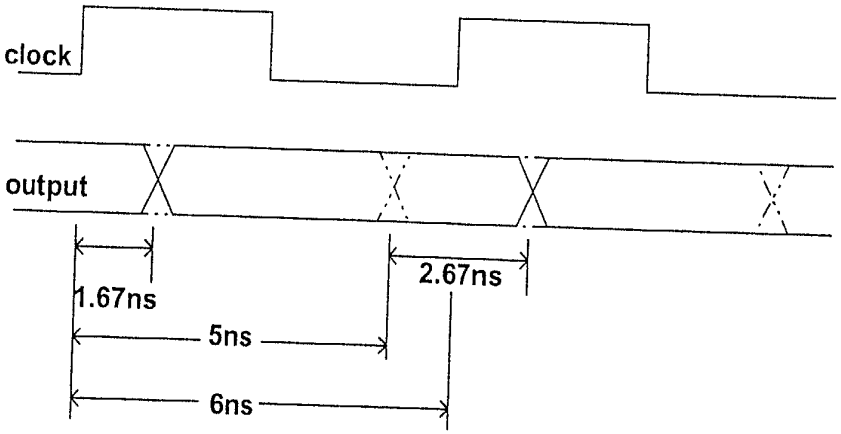


FIGURE 9B

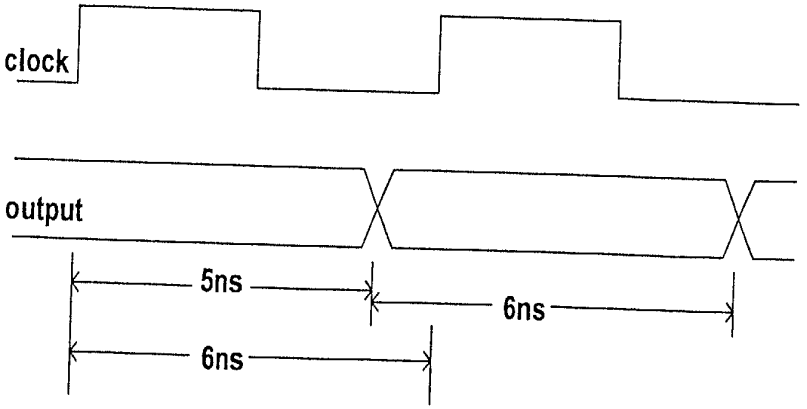


FIGURE 9C

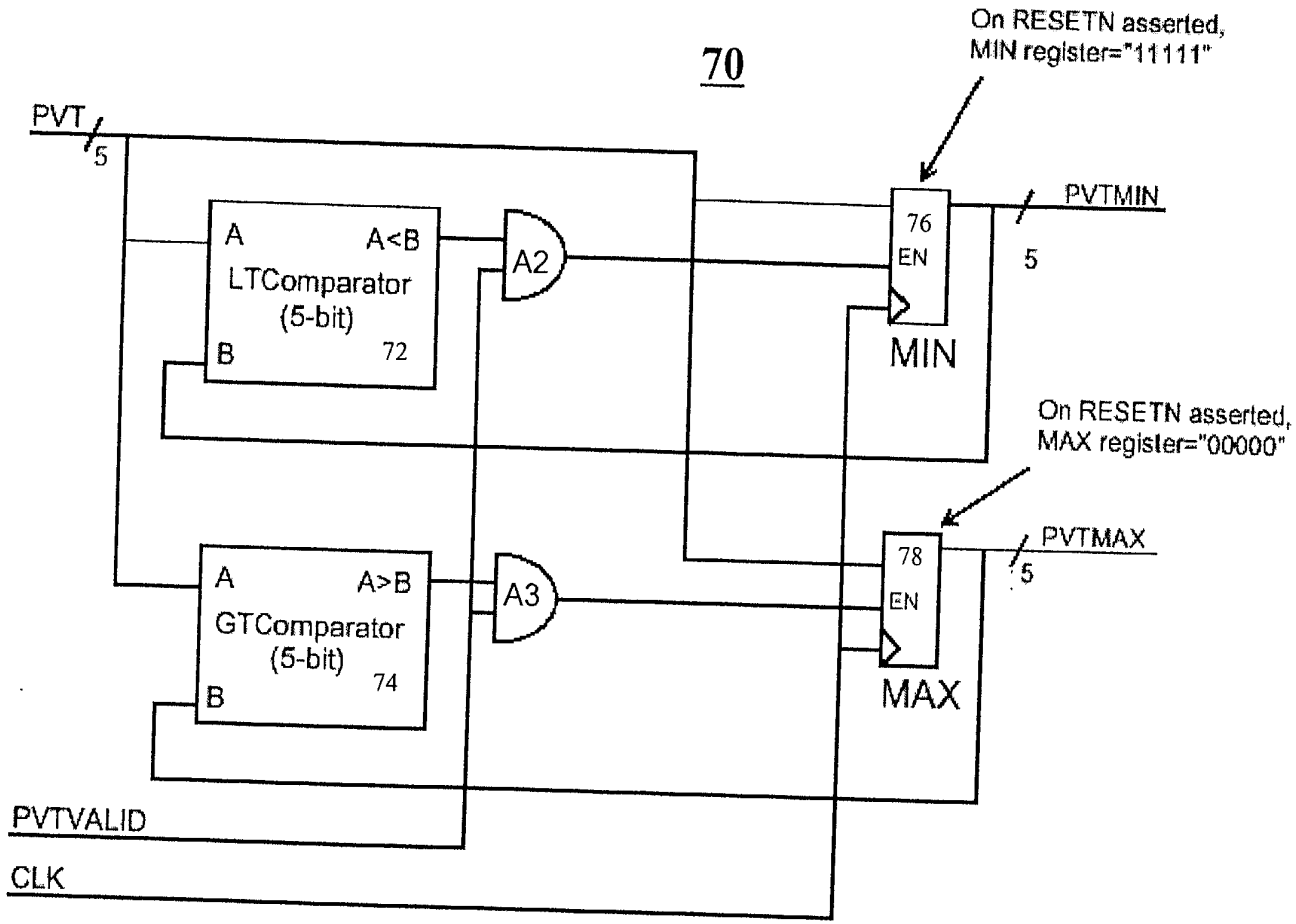


FIGURE 10